REMARKS

Claims 1, 3 and 5 have been amended, claims 2 and 4 have been newly cancelled without any prejudice, and new claims 8-12 have been added. The amendments to the claims and the new claims are fully supported by the originally filed specification, and thus, no new matter is introduced. Reconsideration of pending claims 1, 3 and 5-12 is respectfully requested in view of the following remarks.

Rejection Under 35 USC §103

Claims 1-3 and 6 stand rejected under 35 USC §103(a) as being obvious over US Patent No. 5,381,538 ("Amini") in combination with US Patent No. 5,696,917 ("Mills"). Applicants respectfully traverse the rejection for the following reasons.

Claim 1 has been amended to include features from now cancelled dependent claims 2 and 4. Amended independent claim 1 is directed towards a programmable interface, that includes, among other features,

> a register file having a plurality of registers, ... wherein the plurality of registers includes (i) a general-purpose microcontroller register, (ii) a timer register, (iii) an external input/output (I/O) interface register, (iv) an internal I/O register, (v) a shared register, (vi) an interrupt register, and (vii) a first-in, first-out (FIFO) register configured to communicate with a direct memory access (DMA) controller.

Support for these features may also be found in the originally filed specification, e.g., paragraph 0016 and Fig. 1. Including these registers in the recited register file has several advantages, e.g., allowing the programmable interface to operate as an input/output (I/O) subsystem with minimal overhead on the system processor.[1]

While rejecting similar features in now cancelled claim 2, the Examiner acknowledges that Amini fails to disclose the above recited features. The Examiner, however, alleges that US Patent No. 6,112,275 ("Curry") discloses such features, and refers to Curry's register 2104 of Fig. 21.

Curry's register 2104 is a 8-bit command shift register. "Once command register 2104 is loaded with a command byte, command byte decoder 2106 decodes the command byte to initiate

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[1] Specification, paragraph 0015.

one of the four allowed commands".[2] Thus, the command register 2104 is configured to be loaded with a command byte. However, no where does Curry disclose or even suggest that the command register 2104 includes (i) a general-purpose microcontroller register, (ii) a timer register, (iii) an external input/output (I/O) interface register, (iv) an internal I/O register, (v) a shared register, (vi) an interrupt register, and (vii) a first-in, first-out (FIFO) register configured to communicate with a direct memory access (DMA) controller, as recited in claim 1. In contrast, claim 1 recites a register file that includes all these types of registers.

Although Mills discloses executable codes, the Examiner also has not pointed out where Mills discloses a register file that includes (i) a general-purpose microcontroller register, (ii) a timer register, (iii) an external input/output (I/O) interface register, (iv) an internal I/O register, (v) a shared register, (vi) an interrupt register, and (vii) a first-in, first-out (FIFO) register configured to communicate with a direct memory access (DMA) controller, as recited in claim 1.

Furthermore, claim 1 recites that the programmable interface comprises *a microcontroller* and *a Code Store SRAM configured to bidirectionally communicate with the microcontroller; ... wherein the Code Store SRAM ... [is] configured to bidirectionally communicate with a system processor that is external to the programmable interface*. As the recited microcontroller is included in the programmable interface, and as the recited system processor is external to the programmable interface, this implies that the recited microcontroller and the recited system processor are two different components. Also, the recited code store SRAM communicates bidirectionally with the microcontroller and also with the system processor.

The Examiner alleges that Amini's SRAM 34, microprocessor 30, and processor portion 20 of Fig. 1 disclose the recited SRAM, the recited microcontroller and the recited system processor, respectively. Amini, in Fig. 1, discloses that the processor portion 20 includes the microprocessor 30.[3] That is, Amini's microprocessor 30 is a part of Amini's processor portion 20, as also illustrated in Amini's Fig. 1. As Amini's processor portion 20 includes

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[2] Curry, col. 37, lines 14-17.
[3] Amini, col. 2, line 56.

microprocessor 30, it is physically impossible for Amini's microprocessor 30 to be included in a programmable interface, while Amini's processor portion 20 is external to the programmable interface. Accordingly, it is physically impossible for Amini's microprocessor 30 and processor portion 20 to be equated to the recited microcontroller and the recited system processor, respectively. Accordingly, Applicants respectfully submit that Amini fails to disclose the above recited feature of claim 1.

Furthermore, claim 1 recites that the *microcontroller [is] configured to bidirectionally communicate with the ... run control register; wherein the ... run control register ... [is] configured to bidirectionally communicate with a system processor that is external to the programmable interface.* For at least the above discussed reasons, Amini also does not disclose a run control register that bidirectionally communicates with a microcontroller and also with a run control register.

Moreover, claim 1 recites "executable code, loaded onto the Code Store SRAM; ... wherein the system processor is configured to load the executable code onto the Code Store SRAM and is further configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code." The Examiner alleges that Mills discloses these features. Specifically, the Examiner cites a portion of Mills which states that "[i]n such a case, the program associated with the selected game will be loaded into SRAM 240 . . . . Moreover, the read/write files (including the executable code for the game) stored in battery backed SRAM 240 will not be lost."[4] While this arguably discloses executable code that is stored on SRAM, Applicants respectfully submit that Mills does not disclose a "system processor configured to . . . signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code." (emphasis added). Although the Examiner seems to equate Mills' microprocessor 210 with the recited microcontroller, Mills does not disclose a "system processor" or a "run control register." Even if the executable code stored in SRAM allegedly taught by Mills is combined with the alleged system processor and run control register of Amini, the configuration of the system processor and run control register taught by Amini would not support a "system processor configured to . .

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[4] Mills, col. 10, lines 33-35, 50-52.

. signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code." (emphasis added). Accordingly, Applicants respectfully submit that neither Mills nor Amini, either alone or in combination, disclose this feature.

For at least these reasons, Applicants respectfully submit that independent claim 1 is allowable. Claims 3 and 5-7 depend, either directly or indirectly on claim 1 and therefore, they are allowable for at least the reasons claim 1 is allowable.

New Claims

New claims 8-12 have been added, which depend from claim 1. Support for new claims 8-12 may be found throughout the originally files specification, e.g., in paragraphs 0018, 0019, 0020, 0021 and 0022, respectively, of the originally filed specification. Dependent claims 8-12 are allowable for at least the reasons associated independent claim 1 is allowable.

Conclusion

For at least these reasons, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present paper, the Examiner is kindly requested to contact the undersigned at (503) 796-2997. If any fees are due in connection with filing this paper, the Commissioner is authorized to charge Deposit Account No. 500393.

Respectfully submitted,
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